REMARKS

This is in response to the Office Communication mailed on mailed on June 13, 2007. The only remaining rejection in the Office Action is the rejection of claims 63-91 under 35 U.S.C. §102(b) as being unpatentable over Koyama et al., JP 62-188100. It is respectfully submitted that this rejection is improper, incorrect, and should be withdrawn. As noted in the Preliminary Amendment that was filed concurrently with the present application, claims 63-91 are respectively exact copies of claims 1-17 and 43-54 of U.S. patent number 5,657,270 of Ohuchi *et al.*. The grounds of rejection of claims 63-91 of the present application are ones that would also be equally applicable to claims 1-17 and 43-54 of U.S. patent number 5,657,270. In fact, the Koyama *was* specifically cited by the Examiner during the prosecution U.S. patent number 5,657,270 and this rejection was overcome. Consequently, the Office Action is holding as unpatentable claims 63-91, which are copied from U.S. patent number 5,657,270 for interference purposes, in direct contradiction to what the Patent Office has previously found.

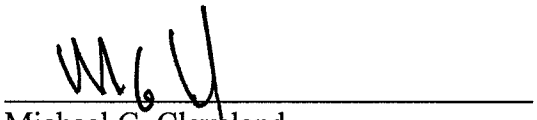
More specifically, the Koyama reference was explicitly cited by the Examiner in the prosecution of U.S. patent number 5,657,270. (More accurately, the application that led to U.S. patent number 5,657,270 was a file wrapper continuation and the reference was cited in the application of which it was a file wrapper continuation.) The Examiner is referred the file history of U.S. patent number 5,657,270 and, specifically, to the entries labeled on the content sheet as "Pre Amdt E" (of 4/3/95, entered on 4/20/95) and as "Pre Amdt F" (of 6/20/95, entered on 7/5/95). Copies of these documents are attached as Exhibits A and B, respectively.

Referring to "Pre Amdt E", the Examiner is referred to the discussion that begins in the first full paragraph of page 13. Referring to "Pre Amdt F" (filed after an intervening interview), the Examiner is referred to the discussion that begins in the first full paragraph of page 14. These remarks were found persuasive. (There were no subsequent rejections on prior art before claims 1-17 and 43-54 of U.S. patent number 5,657,270 were allowed.) Consequently, a rejection of claims 63-91 (which are exact copies of claims 1-17 and 43-54 of U.S. patent number 5,657,270) under 35 U.S.C. §102(b) on Koyama is directly contrary to the previous findings of the Patent Office and, in effect, would be declaring the claims of an issued patent as not allowable.

On the basis of the arguments given with respect to U.S. patent number 5,657,270, it is respectfully submitted that a rejection of claims 63-91 is not well founded. Further, it is again noted that this rejection is improper and premature.

In particular, the Examiner is referred to item 6 of section 1003 of the M.P.E.P. that lists matters that are to be submitted to the Technology Center Directors. As stated there, these matters include: "6. Actions which hold unpatentable claims copied from a patent for interference purposes where the grounds relied upon are equally applicable to the patentee". As discussed above (and in the last several Responses), this is the case of the prior art rejection given in the Office Action; therefore, the rejection must have the approval of the TC Director. Since the Office Action in the present application has not provided this special approval, the rejection is consequently improper and should therefore be withdrawn.

Respectfully submitted,



12/07/07

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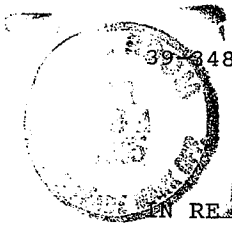
EXHIBIT A
PRELIMINARY AMENDMENT "E" OF APRIL 3, 1995,
ENTERED APRIL 20, 1995.



22/E
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BCM

39-3486-2 SRD FWC I

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

KAZUNORI OHUCHI ET AL. : GROUP ART UNIT: 2503

SERIAL NO: 08/376,665 :

FILED: JANUARY 23, 1995 : EXAMINER: CRANE

FOR: ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY WITH THRESHOLD VALUE CONTROLLER FOR DATA PROGRAMMING

PRELIMINARY AMENDMENT

HONORABLE COMMISSIONER OF PATENTS & TRADEMARKS
WASHINGTON, D.C. 20231

SIR:

Prior to examination on the merits of the present Rule 62 File Wrapper Continuation Application, please amend this application as follows:

IN THE CLAIMS

Please cancel without prejudice pending Claims 48-57 and substitute therefore new Claims 58-97 as follows:

E1 Amd F1

--58. A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells, each including a transistor with a charge storage portion;

a plurality of data storage circuits for storing data to directly control write voltages applied to said memory cells;

a write circuit for simultaneously applying said write voltages to said memory cells according to said data stored in said data storage circuits; and

a plurality of data control circuits ~~for partially modifying said data stored in said data storage circuits~~ based on said data stored in said data storage circuits and actual written states of said memory cells, such that only memory cells which are not correctly written are correctly written.

59. The device according to Claim 58, wherein said data stored in said data storage circuit are initially set to initial data, and then said initial data stored in said data storage circuits are modified by said data control circuits.

~~60.~~ The device according to Claim ~~59~~, wherein said initial data are loaded from at least one input line.

61. The device according to Claim 58, further comprising a monitor circuit for simultaneously monitoring said actual written states of said memory cells.

62. The device according to Claim 58, wherein said data stored in said data storage circuits are modified partially and simultaneously by said data control circuit.

63. The device according to Claim 58, wherein said data control circuit includes bit line voltage regulation circuits for selectively changing voltages of said bit lines according to said data stored in said data storage circuits.

64. The device according to Claim 63, wherein said voltages of bit lines are changed selectively and simultaneously by said bit line voltage regulation circuits.

65. The device according to Claim 58, wherein said modifying of said data stored in said data storage circuits and said applying said write voltages according to said data stored in said data storage circuits are repeated until all of accessed memory cells are sufficiently programmed.

66. The device according to Claim 58, wherein said modifying of said data stored in said data storage circuits and said applying said write voltages according to said data stored in said data storage circuits are repeated during a limited number of cycles.

67. The device according to Claim 58, wherein said data storage circuits and said data control circuit is arranged on said semiconductor substrate.

68. The device according to Claim 67, wherein said data storage circuits are arranged adjacent to said memory cell array.

69. The device according to Claim 58, wherein each of said data storage circuits is connected to a respective one of said bit lines.

70. The device according to Claim 58, further comprising a verify-termination detector for detecting whether or not all of accessed memory cells are sufficiently programmed.

71. The device according to Claim 70, wherein said verify-termination detector is arranged on said semiconductor substrate.

72. The device according to claim 58, wherein said write circuit is formed of a plurality of write circuits.

73. A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells, each including a transistor with a charge storage portion;

a plurality of data storage circuits for storing data to control write voltages applied to said memory cells, said data being initially set to initial data which are loaded from at least one input line;

a write circuit for simultaneously applying said write voltages to said memory cells according to said data stored in said data storage circuits; and

a data control circuit for partially modifying said initial data stored in said data storage circuits based on said data stored in said data storage circuits and actual written states of said memory cells, such that only memory cells which are not correctly written are correctly written.

74. The device according to Claim 73, further comprising a monitor circuit for simultaneously monitoring said actual written states of said memory cells.

75. The device according to Claim 73, wherein said data stored in said data storage circuits are modified partially and simultaneously by said data control circuits.

76. The device according to Claim 73, wherein said data control circuits include bit line voltage regulation circuits for selectively changing voltages of said bit lines according to said data stored in said data storage circuits.

77. The device according to Claim 76, wherein said voltages of bit lines are changed selectively and simultaneously by said bit line voltage regulation circuits.

78. The device according to Claim 73, wherein said modifying of said data stored in said data storage circuits and said applying said write voltages according to said data stored in said data storage circuits are repeated until all of accessed memory cells are sufficiently programmed.

79. The device according to Claim 73, wherein said modifying of said data stored in said data storage circuits and said applying said write voltages according to said data stored in said data storage circuits are repeated during a limited number of cycles.

80. The device according to Claim 73, wherein said data storage circuits and said data control circuits are arranged on said semiconductor substrate.

81. The device according to Claim 80, wherein said data storage circuits are arranged adjacent to said memory cell array.

82. The device according to Claim 73, wherein each of said data storage circuits is connected to a respective one of said bit lines.

83. The device according to Claim 73, further comprising a verify-termination detector for detecting whether or not all of accessed memory cells are sufficiently programmed.

84. The device according to Claim 83, wherein said verify-termination detector is arranged on ~~said~~ semiconductor substrate.

85. A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells, each including a transistor with a charge storage portion;

a plurality of program circuits including a plurality of write circuits for simultaneously writing data into said memory cells and a plurality of verify circuits for simultaneously verifying actual written states of said memory cells;

a plurality of data storage circuits for storing write control data to control write voltages applied to said memory cells and for selectively sensing said actual written states with said verify circuits, based on said write control data and for selectively keeping said write control data during program operation with said program circuits and for storing sensed data as said write control data.

86. The device according to Claim 85, wherein said data stored in said data storage circuits are initially set to initial data.

87. The device according to Claim 86, wherein said initial data are loaded from at least one input line.

88. The device according to Claim 85, wherein said data storage circuits simultaneously sense said actual written states of said memory cells.

89. The device according to Claim 85, further comprising bit line voltage regulation circuits for selectively changing voltages of said bit lines according to said write control data stored in said data storage circuits.

90. The device according to Claim 89, wherein said bit line voltage regulation circuits simultaneously change voltages of said bit lines according to said write control data stored in said data storage circuits.

91. The device according to Claim 85, wherein said writing, sensing, and verifying are repeated until all of accessed memory cells are sufficiently programmed.

92. The device according to Claim 85, wherein said writing, sensing, and verifying are repeated during a limited number of cycles.

93. The device according to Claim 85, wherein said data storage circuits and said program circuits are arranged on said semiconductor substrate.

94. The device according to Claim 85, wherein said data storage circuits are arranged adjacent to said memory cell array.

95. The device according to Claim 85, wherein each of said data storage circuits is connected to a respective one of said bit lines.

96. The device according to Claim 85, wherein each of said data control circuits including a verify-termination detector.

97. The device according to Claim 96, wherein each of said verify-termination detectors is arranged on said semiconductor substrate.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Newly submitted Claims 58-97 are presently active in this case, Claims 48-57 having been cancelled by way of the present amendment, and Claims 1-47 having previously been cancelled.

In the parent application, Claims 48-57 were rejected under 35 U.S.C. §103 as being unpatentable over the IBM Technical Disclosure Bulletin, "EPROM" Programming Device" (hereinafter called "IBM"), Koyama et al (JP 62-188,100) and Momodomi et al ('690), considered together. As understood by Applicants, the outstanding rejection in the parent application was based on the findings, summarized as follows:

> "The IBM Bull. teaches explicitly the steps of programming, reading, comparing, verifying, altering of data in response to the verify step, and retrying. The reference does not state whether these steps are performed bit-by-bit or not. Koyama teaches compare, verify, and alteration steps performed bit-by-bit. It would be obvious to perform the IBM steps bit-by-bit as taught by Koyama et al., so that the repeated process of a rewrite until proper readout becomes possible, as desired by Koyama et al.
>
> The IBM teaching is to verify and alter, continuing to completion, retry, or display or error. Clearly the intent is to stop testing once a bit meets the verification criterion, leaving a cell undisturbed if its threshold voltage is correct. Alternatively, it would be obvious to stop testing once a bit meets the verification criterion, because otherwise one would never finish programming the EPROM.
>
> Also, since Momodomi et al. teaches an EPROM that must be programmed, and presumably programmed correctly, there is no impossibility associated with combining the Momodomi teaching with the IBM teaching of a verification procedure."

Applicants respectfully traverse the findings as above-stated because in Applicants' view these findings are based on a misunderstanding of Applicants' invention and on a misunderstanding about EPROM techniques. The applicants thus

have prepared the following comments in order to overcome the prior rejection:

First, Applicants address the IBM reference.

The program disclosed in the IBM reference is executed for each of the bytes (page 4145, line 16). In a verifying method executed for each of the bytes, the writing operation and the verifying operation are repeatedly executed until all of the data of 1 byte (usually, 8 bits) are written in the memory cells, without changing the data. Thus, according to the verifying method as described in IBM, when the data is not completely written in one of the memory cells, the writing operation of the same data is continuously repeated for all memory cells of 1 byte. In this time, the writing operation may be further and excessively executed for the cell in which the data have been sufficiently written (see attached EXHIBIT B(1)). However, even if the data is excessively written in the cell, no problem will occur. This is because, the writing threshold voltage of the cell of the EPROM is usually set in the region indicated as "write" in the attached EXHIBIT A (i.e., larger than Vcc, for example). The data stored in the cell of EPROM are simultaneously erased by ultraviolet rays. The erasing threshold voltage of the cell of the EPROM is thus stably set in the region indicated as "erase" in the EXHIBIT A. Therefore, in the conventional semiconductor device, any trouble or problem due to the verifying method executed for each of the bytes as disclosed in IBM will not occur.

In recent years, however, highly precise control of the threshold voltage is required not for each of the bytes but for each of cells (bits). Applicants' invention intends to provide a device for realizing this precise control. Applicants' invention intends to provide a non-volatile semiconductor memory device for preventing the above-mentioned excessive writing of the data in the memory cell and for verifying the writing condition cell-by-cell, and thus differs from the device disclosed in IBM using the verifying method executed for each of the bytes.

The outstanding Office Action in the parent application states that the altering of data in response to the verifying step is taught in IBM. Nevertheless IBM makes no reference to the data altering. In IBM it is stated that IBM relates "particularly, to apparatus for altering a variety of electrically programmable read-only memories (EPROMs)" (page 4145, lines 1-3), and that "an EPROM thus can be mounted on the personal computer without the need of cover removal" (lines 8-9). However, IBM does not teach the data altering in response to the verifying step as suggested by the Examiner. In the device of IBM an EPROM itself is altered.

In the device of IBM, the programming results are read back to the personal computer and compared (lines 17-18). However, concerning the processes following the comparing process, IBM. merely describes that the program continues to completion, retries or display of error information (lines 19-20), and does not provide any specific teaching.

Still less, IBM does not disclose, unlike Applicants' invention, to partially modify data latched by a data storage circuit in accordance with the actual written states of said memory cells and the data stored in the data storage circuit.

In Applicants' invention, the data written in the cell are verified for each of the cells so as to be updated. According to Applicants' invention, the writing threshold voltage can be maintained in a predetermined region (OV to Vcc, for example) as shown in the EXHIBIT B(2), and thus the excessive writing of the data in the memory cell as aforementioned will not occur. By virtue of this feature, the reliability of writing will increase without shortening the durability of the memory cells.

The above-mentioned partially modifying of the written data is an important feature of Applicants' invention. The data control circuit executes the partial modifying of write data. The specific description about the partial modifying of the data stored in the data storage circuit by a data control circuit is not disclosed in IBM.

The prior rejection has further stated concerning IBM, that "it would be obvious to stop testing once a bit meets the verification criterion, because otherwise one would never finish programming the EPROM". Applicants' disagree with this finding. In an EPROM shown in the enclosed data books "Bipolar/MOS Memories 1986" (particularly in Fig. 1) and "SEEQ DATA BOOK 1988/89" (particularly in page 3-5, flowchart) which have been published at substantially the same time as programming is repeatedly executed for memory cells of one

byte non-selectively until it is determined that data is correctly written in all of the memory cells of one byte, or repeated predetermined times. In the program disclosed in IBM, wherein the verifying operation is executed for each of the bytes, the verifying operation is not executed for one cell (one bit). While, in Applicants' invention, the program verifying operation is selectively executed for each of the memory cells. Therefore, the verifying operation of Applicants' invention differs from that of IBM, or the data books.

Turning now to Koyama et al, this reference relates to a method for writing data in a memory cell, which is suitable for a preprocessing of a storage characteristic test. In order to maintain the threshold voltage of bits over a constant level, Koyama et al execute a verifying operation for each of cells. Koyama et al, however, do not teach the verifying operation for each of cells during the normal writing operation.

The verifying operation for each of cells of Koyama et al will be briefly described below.

Koyama et al show in Fig. 2 circuits 3_1 to 3_n for comparing data written in EPROM with write data signal D_1 to D_n. In these circuits, EX-OR circuit 51 determines whether or not signal 101a and readout data signal 11a coincide with each other, and if the signals do not coincide with each other, data is rewritten in the EPROM till the signals coincide with each other. When the signals coincide with each other, the output from OR circuit 101, i.e., the signal 101a, changes

from "O" to "1" and the signal 101a of "1" is written in the same bit.

Differences between Koyama et al and Applicants' invention are as follows:

(1) The memory cell in Koyama et al do not have a circuit for storing (or latching) data. Still less, Koyama et al do not disclose a circuit for partially modifying the data;

(2) Since the data cannot be stored, the CPU must continue to send data to the EPROM during programming or verifying. Therefore, the CPU cannot execute any other operations during programming or verifying; and

(3) Since the data cannot be stored, the number of the memory cells which can be programmed or verified at the same time is the same as the number of bits corresponding to the width of the external bus (i.e., the number of bits corresponding to the number of buses shown in Fig. 2, 2_1 to 2_n). In other words, the number of the memory cells which can be programmed or verified at the same time is the same as the number of cells of 1 byte (n bits) defined by one address. The same may be said of the IBM device.

Further, the circuit 71 of Koyama et al is a flip-flop circuit which latches not data but a control signal for determining whether or not the write data signal supplied to terminal 111 should pass through the OR circuit 101. The changes of the output value of the circuit 101 do not indicate that the circuit 101 updates data in accordance with the written state of the memory cell. The write data D1 is not changed and the circuit 101 merely controls the passing of the

data D1. Also, if the CPU is to execute any other operations during programming or verifying, two circuits are needed to execute the verifying operation, i.e., a circuit for latching write data signal which is input to the terminal 111 (in Koyama et al, an external CPU is supposed to be corresponded), for example, and a flip-flop circuit 71 (the operation of the two circuits are shown in Fig. 3 as "write data signal D1" and "71 output"). In order to constitute the above-mentioned structure of Koyama et al on one chip, the occupied area of the whole circuits is inevitably increased. In addition, when a program of 1 byte defined by one address is finished and the program of the next address starts, the driver comparator circuit 31 of Koyama et al cannot correctly operate merely by being supplied a new address signal and write data signal. This is because, the OR gate 101 is prohibited from operating and the write data signal cannot pass the OR gate 101. In order to operate the driver comparator circuit 31 correctly, a clear signal supplied from control signal line 8 must be input in order to reset the flip-flop circuit 71, with the result that the operation is so complicated.

In contrast, the data storage circuit of the present invention has the following advantages over Koyama et al:

(1) The single and simple circuit has the same function as the verification function of Koyama et al which is realized by the external circuit for latching the write data signal and the flip-flop circuit 71, and thus can decrease the occupied area on one chip. In addition, according to Applicants' invention, when a program defined by one address (in

Applicants' invention, of a plurality of bytes) is finished, the next program can easily start merely by being supplied a new address signal and write data signal.

(2) The device of Applicants' invention includes the data storage circuit and data control circuit, and thus the CPU can execute another operation after sending the program data to the EEPROM, since the data control circuit automatically and partially modifies the write data.

(3) The device of Applicants' invention comprises a plurality of data storage circuits. Therefore, the data of a plurality of addresses are repeatedly transferred from the CPU to the data storage circuit, and data of a plurality of bytes latched in the data storage circuit can be simultaneously programmed and verified. With this structure, high-speed processing can be attained.

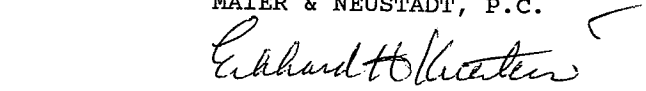
As described above, even if IBM and Koyama et al are combined in any manner, the data control circuit of the present invention which partially modifies the data stored in the data storage circuit on the basis of the stored data and the data actually written in memory cells cannot be inferred from the combination of the references. Similarly, even if Momodomi discloses an EEPROM, it is respectfully submitted that the finding that Applicants' invention can be obtained from the combination of Momodomi and IBM, is not correct, since, as aforementioned, IBM, does not disclose the specific verifying of memory cells.

Accordingly, in light of the newly submitted claims, and in view of the above discussion, the newly submitted claims

are believed patentably distinguishing over the prior art applied in the parent application, and in condition for allowance. An early and favorable action to that effect is therefore respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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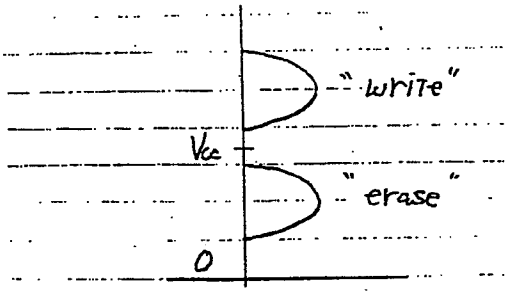
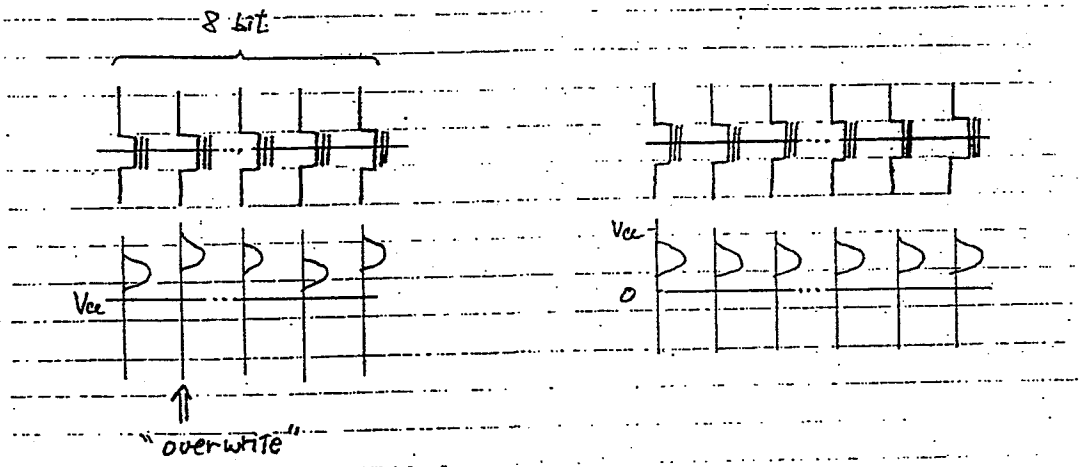
[EXHIBIT A]



IBM.

[EXHIBIT B]



(2) IBM

(2) INVENTION

EXHIBIT B
PRELIMINARY AMENDMENT "F" OF JUNE 20, 1995,
ENTERED JULY 5, 1995.

39-3486-2 SRD FWC I

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

KAZUNORI OHUCHI ET AL. : GROUP ART UNIT: 2503

SERIAL NO: 08/376,665 :

FILED: JANUARY 23, 1995 : EXAMINER: CRANE

FOR: ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY WITH THRESHOLD VALUE CONTROLLER FOR DATA PROGRAMMING

SUPPLEMENTAL PRELIMINARY AMENDMENT

HONORABLE COMMISSIONER OF PATENTS & TRADEMARKS
WASHINGTON, D.C. 20231

SIR:

Prior to examination on the merits of the present Rule 62 File Wrapper Continuation Application, and supplemental to the preliminary amendment filed April 3, 1995, please amend this application as follows:

IN THE CLAIMS

Please cancel without prejudice Claim 72.

Please amend Claims 58-59, 61-70, 73-83, 85-86, and 88-96 as follows:

--58. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells, each including a transistor with a charge storage portion;

[a plurality of data storage circuits for storing data to directly control write voltages applied to said memory cells;

a write circuit for simultaneously applying said write voltages to said memory cells according to said data stored in said data storage circuits; and

a plurality of data control circuits for partially modifying said data stored in said data storage circuits based on said data stored in said data storage circuits and actual written states of said memory cells, such that only memory cells which are not correctly written are correctly written]

a plurality of programming control circuits for storing data defining control write voltages to be applied to respective of said memory cells, for simultaneously applying said control write voltages to said respective of said memory cells according to the data stored by said plurality of programming control circuits, for determining actual written states of said memory cells, and for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored by said plurality of programming control circuits, such that only memory cells which are not sufficiently written have been applied with control write voltages which achieve a predetermined written state in the respective memory cell.

59. (Amended) The device according to Claim 58, wherein said data stored in said [data storage] programming control circuits are initially set to initial data, and then said initial data stored in said [data storage] programming control circuits are modified [by said data control circuits] in accordance with said predetermined logical relationship.

61. (Amended) The device according to Claim 58, [further comprising a monitor for] wherein said plurality of programming control circuits simultaneously [monitoring] determine said actual written states of said memory cells.

62. (Amended) The device according to Claim 58, wherein said data stored in said [data storage] plurality of programming control circuits are modified [partially and] simultaneously [by said data control circuit] in accordance with said predetermined logical relationship.

63. (Amended) The device according to Claim 58, wherein said [data] programming control circuits include[s bit line voltage regulation circuits] means for selectively changing voltages of said bit lines according to said data stored in said [data storage] programming control circuits.

64. (Amended) The device according to Claim 63, wherein said voltages of bit lines are changed selectively and simultaneously by said [bit line voltage regulation circuits] means for selectively changing voltages to said bit lines.

65. (Amended) The device according to Claim 58, wherein [said] selective modifying of said data stored in said [data storage] programming control circuits and [said] applying said control write voltages [according to said data stored in said

[data storage circuits are repeated] to said respective of said memory cells are continued until [all of accessed] each memory cell[s are] is sufficiently [programmed] written.

66. (Amended) The device according to Claim 58, wherein [said] modifying of said data stored in said [data storage] programming control circuits and [said] applying said control write voltages according to said data stored in said [data storage] programming control circuits are repeated during a limited number of cycles.

67. (Amended) The device according to Claim 58, wherein said [data storage] programming control circuits [and said data control circuit is] are arranged on said semiconductor substrate.

68. (Amended) The device according to Claim 67, wherein said [data storage] programming control circuits are arranged adjacent to said memory cell array.

69. (Amended) The device according to Claim 58, wherein each of said [data storage] programming control circuits is connected to a respective one of said bit lines.

70. (Amended) The device according to Claim 58, further comprising a verify-termination detector for detecting whether or not all of [accessed] said memory cells are sufficiently programmed in accordance with the modified data in said programming control circuits based on a predetermined logical relationship.

73. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells, each including a transistor with a charge storage portion; and

[a plurality of data storage circuits for storing data to control write voltages applied to said memory cells, said data being initially set to initial data which are loaded from at least one input line;

a write circuit for simultaneously applying said write voltages to said memory cells according to said data stored in said data storage circuits; and

a data control circuit for partially modifying said initial data stored in said data storage circuits based on said data stored in said data storage circuits and actual written states of said memory cells, such that only memory cells which are not correctly written are correctly written]

a plurality of programming control circuits for storing data defining control write voltages to be applied to respective of said memory cells, said data being initially set to initial data which are loaded from at least one input line, for simultaneously applying said control write voltages to said respective of said memory cells according to the data stored by said plurality of programming control circuits, for determining actual written states of said memory cells, and for selectively modifying said stored data based on a predetermined logical relationship between the determined

actual written states of said memory cells and the actual data stored by said plurality of programming control circuits, such that only memory cells which are not sufficiently written have been applied with control write voltages which result in charge storage in the charge storage portion of the respective memory cell.

74. (Amended) The device according to Claim 73, [further comprising a monitor for] wherein said plurality of programming control circuits simultaneously [monitoring] determine said actual written states of said memory cells.

75. (Amended) The device according to Claim 73, wherein said data stored in said [data storage] programming control circuits are modified [partially and] simultaneously [by said data control circuits] in accordance with said predetermined logical relationship.

76. (Amended) The device according to Claim 73, wherein said [data control] programming control circuits include [bit line voltage regulation circuits] means for selectively changing voltages of said bit lines according to said data stored in said [data storage] programming control circuits.

77. (Amended) The device according to Claim 76, wherein said voltages of said bit lines are changed [selectively and] simultaneously by said [bit line voltage regulation circuits] means for selectively changing voltages of said bit lines.

78. (Amended) The device according to Claim 73, wherein [said] selective modifying of said data stored in said [data storage] programming control circuits and [said] applying said control write voltages [according to said data stored in said

data storage circuits] to said respective of said memory cells are continued [are repeated] until [all of accessed] each memory cell[s are] is sufficiently [programmed] written.

79. (Amended) The device according to Claim 73, wherein [said] selective modifying of said data stored in said [data storage] programming control circuits and [said] applying said control write voltages [according to said data stored in said data storage circuits are repeated during] to said respective of said memory cells are repeated during a limited number of cycles.

80. (Amended) The device according to Claim 73, wherein said [data storage circuits and said data control] programming control circuits are arranged on said semiconductor substrate.

81. (Amended) The device according to Claim 80, wherein said [data storage] programming control circuits are arranged adjacent to said memory cell array.

82. (Amended) The device according to Claim 73, wherein each of said [data storage] programming control circuits is connected to a respective one of said bit lines.

83. (Amended) The device according to Claim 73, further comprising a verify-termination detector for detecting whether or not all of accessed memory cells are sufficiently [programmed] written.

85. (Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells, each including a transistor with a charge storage portion;

a plurality of programming control circuits [including a plurality of write circuits for simultaneously writing data into said] for controlling selection of memory cells, [and] application of write voltages to the selected memory cells and application of verify voltages to the selected memory cells for sensing [a plurality of verify circuits for simultaneously verifying] actual written states of said memory cells;

a plurality of data [storage] circuits for storing write control data of first and second logic levels which [to] control write voltages to be applied to respective of said memory cells selected by said programming control circuits, for applying said write voltages to respective of said memory cells, [and] for selectively sensing [said] actual written states [with said verify circuits, based on said write control data and for selectively keeping said write control data during program operation with said program circuits and for storing sensed data as said write control data] of only those of said respective memory cells corresponding to data circuits in which write control data of said first predetermined logic level are stored, for modifying stored write control data from said first predetermined logic level to said second predetermined logic level in those data circuits corresponding to memory cells in which successful writing of data has been

sensed, for maintaining said stored write control data at said first predetermined logic level in the data circuits corresponding to the memory cells in which data has not been successfully written, and for maintaining said stored write control data at said second predetermined logic level in the data circuits storing said predetermined second logic level.

86. (Amended) The device according to Claim 85, wherein said data stored in said data [storage] circuits are initially set to initial data.

88. (Amended) The device according to Claim 85, wherein said data [storage] circuits simultaneously sense said actual written states of said memory cells.

89. (Amended) The device according to Claim 85, further comprising [bit line voltage regulation circuits] means for selectively changing voltages of said bit lines according to said write control data stored in said data [storage] circuits.

90. (Amended) The device according to Claim 89, wherein said means for selectively changing voltages of said bit lines [voltage regulation circuits] simultaneously change voltages of said bit lines according to said write control data stored in said data storage circuits.

91. (Amended) The device according to Claim 85, wherein said [writing] applying, sensing, and [verifying] modifying [are repeated] are continued until [all of accessed] each of said memory cells [are] is sufficiently [programmed] written.

92. (Amended) The device according to Claim 85, wherein said [writing] applying, sensing, and [verifying] modifying are repeated during a limited number of cycles.

93. (Amended) The device according to Claim 85, wherein said data [storage] circuits and said programming control circuits are arranged on said semiconductor substrate.

94. The device according to Claim 85, wherein said data [storage] circuits are arranged adjacent to said memory cell array.

95. (Amended) The device according to Claim 85, wherein each of said data [storage] circuits is connected to a respective one of said bit lines.

96. (Amended) The device according to Claim 85, wherein each of said data [control] circuits [including] includes a verify-termination detector.---

Please add new claims 98-111 as follows:

--98. The device according to claim 58, in which said plurality of programming control circuits selectively modify said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells after application of control write voltages thereto and the actual data stored by said plurality of programming control circuits prior application of said control write voltage.

99. The device according to claim 73, in which said plurality of programming control circuits selectively modify said stored data based on a predetermined logical relationship between the determined actual written states of said memory

cells after application of control write voltages thereto and the actual data stored by said plurality of programming control circuits prior application of said control write voltage.

100. A system including a non-volatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells, each including a transistor with a charge storage portion; and

a plurality of programming control circuits for storing data defining control write voltages to be applied to respective of said memory cells, said data being initially set to initial data which are loaded from at least one input line, for simultaneously applying said control write voltages to said respective of said memory cells according to the data stored by said plurality of programming control circuits, for determining actual written states of said memory cells, and for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored by said plurality of programming control circuits, such that only memory cells which are not sufficiently written have been applied with control write voltages which result in charge

storage in the charge storage portion of the respective memory cell.

101. The system according to Claim 100, wherein said plurality of programming control circuits simultaneously determine said actual written states of said memory cells.

102. The system according to Claim 100, wherein said data stored in said programming control circuits are modified simultaneously in accordance with said predetermined logical relationship.

103. The system according to Claim 100, wherein said programming control circuits include means for selectively changing voltages of said bit lines according to said data stored in said programming control circuits.

104. The system according to Claim 103, wherein said voltages of bit lines are changed simultaneously by said means for selectively changing voltages of said bit lines.

105. The system according to Claim 100, wherein selective modifying of said data stored in said programming control circuits and applying said control write voltages to said respective of said memory cells are continued until each memory cell is sufficiently written.

106. The system according to Claim 100, wherein selective modifying of said data stored in said programming control circuits and applying said control write voltages to said respective of said memory cells are repeated during a limited number of cycles.

107. The system according to Claim 100, wherein said programming control circuits are arranged on said semiconductor substrate.

108. The system according to Claim 107, wherein said programming control circuits are arranged adjacent to said memory cell array.

109. The system according to Claim 100, wherein each of said programming control circuits is connected to a respective one of said bit lines.

110. The system according to Claim 100, further comprising a verify-termination detector for detecting whether or not all of accessed memory cells are sufficiently written.

111. The system according to Claim 110, wherein said verify-termination detector is arranged on a semiconductor substrate.--

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 58-71, and 73-111 are presently active in this case, Claim 72 having been cancelled, claims 58-59, 61-70, 73-83, 85-86, and 88-96 having been amended, and claims 98-111 having been added by way of the present amendment.

Applicants acknowledge with appreciation the courtesy of an interview granted to Applicants on May 22, 1995, at which time the issues outstanding in the parent application were

discussed and at which time the operation of the sensing/latching circuit that controls writing of memory cells was explained. No agreement was reaching, Applicants' attorney indicating that a Supplemental Preliminary Amendment revising the claims would be submitted in the present application.

In the parent application, Claims 48-57 were rejected under 35 U.S.C. §103 as being unpatentable over the IBM Technical Disclosure Bulletin, "EPROM" Programming Device" (hereinafter called "IBM"), Koyama et al (JP 62-188,100) and Momodomi et al ('690), considered together. As understood by Applicants, the outstanding rejection in the parent application was based on the findings, summarized as follows:

> "The IBM Bull. teaches explicitly the steps of programming, reading, comparing, verifying, altering of data in response to the verify step, and retrying. The reference does not state whether these steps are performed bit-by-bit or not. Koyama teaches compare, verify, and alteration steps performed bit-by-bit. It would be obvious to perform the IBM steps bit-by-bit as taught by Koyama et al., so that the repeated process of a rewrite until proper readout becomes possible, as desired by Koyama et al.
>
> The IBM teaching is to verify and alter, continuing to completion, retry, or display or error. Clearly the intent is to stop testing once a bit meets the verification criterion, leaving a cell undisturbed if its threshold voltage is correct. Alternatively, it would be obvious to stop testing once a bit meets the verification criterion, because otherwise one would never finish programming the EPROM.
>
> Also, since Momodomi et al. teaches an EPROM that must be programmed, and presumably programmed correctly, there is

> no impossibility associated with combining the Momodomi teaching with the IBM teaching of a verification procedure."

Applicants respectfully traverse the findings as above-stated for the reasons noted in the Preliminary Amendment filed on April 3, 1995. Nevertheless, in view of the above claim amendments, and in light of the discussions during the May 22, 1995 discussions with the Examiner, the following clarification and explanation of Applicants' invention is further provided in order to assist the Examiner in the evaluation of patentability in the pending amended claims.

The pending claims are drafted with a breadth to cover two embodiments of Applicants' invention as disclosed in Figure 6 and Figure 11. In Figure 6, dedicated storage circuits 16 latch control write data and in which dedicated sensing circuits 18 sense the actual written states of the memory cells and circulate the sensed actual written states via the circuits 22 back to the latch circuits 16 to alter the control write data stored in the latch circuits 16 in accordance with a predetermined logical relationship between the sensed actual written states of the plurality of the memory cells and the actual data in the latch circuits 16. In Figure 11, on the other hand, bit line controllers 162 and 164 operate as latch/sense circuits which alternately perform the latch function and the sensing function, respectively. For example, if it is assumed that the control write data are stored in the controller 162 of Figure 11, and are written from the controller 162 into the memory cells of the array

152, then the circuits of the controller 164 serve as sensing amplifiers which have stored previous control write data. In this embodiment, if a memory cell is successfully written, the successful writing is sensed by the controller operating as a sensing circuit, in the example given by the controller 164, with the controller 164 then modifying the write control data stored therein and then serving as the source of write control data next to be applied to the memory array. In the next iteration, control data stored in the controller 164 are applied to the memory cell array, the actual written states of the memory cells of the array are then sensed by the controller 162, such that for those memory cells having a written state changed from the preceding iteration, the change is sensed by the controller 162 which then has the write control data previously stored therein changed to reflect the successful programming with respect to the particular memory cell.

Thus, while Figure 6 shows a circulating embodiment which control data is latched in the latch 16 and actual written state is sensed by the sensor 18 and the modified control data is circulated back to the latch 16 through the circuit 22, Figure 11 shows a "ping-pong" embodiment in which the function of "latching/sensing" or "sensing/latching" are alternated between the controllers 162 and 164.

In either of the Figure 6 and Figure 11 embodiments, addressed memory cells are programmed simultaneously. Before an initial program operation, all of addressed cells are erased to be, for example, in the logic "0" state. Initial

data from input lines are then stored in the latch 16 of Figure 6 or the controller 162 of Figure 11. The programming operation is then implemented by applying write control voltages to respective memory cells based on the logic level of stored control data. Successful writing/programming is then verified and writing iterations continue until successful writing into the respective memory cells is completed.

In implementing actual writing to respective memory cells, a word line write voltage (for example, about 20V) is applied to an addressed word line WL. For those data circuits storing, for example, a logic "1"-write control data, voltages of corresponding bit lines are set to a first bit line write voltage, for example 0 V. The potential difference between the word line and the bit line is thus 20 V, and due to this large potential difference charge is stored in the floating gate of the respective memory cell. Where sufficient charge is stored, the corresponding memory cell changes from an erased state (logic "0"-state) to a logic "1"-state. For those other data circuits which store logic "0" write control data, corresponding bit lines are raised to a second bit line write voltage, for example 8 V. In this case, the state of the corresponding memory cells is not changed, because the potential difference between the word line and the bit line is not sufficient to cause further charge storage on the floating gate and thus not enough to change the state of the respective cell. Such memory cells remain in the erased (logic "0") state.

After a write operation in which write voltages corresponding to the write control data stored in the data circuits has been applied to the memory cells, the actual written states of the memory cells is sensed. In those memory cells in which it is sensed that the written state has changed from a logic "0"-state to a logic "1"-state, the write control data corresponding to that cell are changed from a logic "1" to a logic "0", thereby to avoid further writing into those memory cells, i.e., to avoid further charging of charge onto the floating gate of those memory cells. For those memory cells having applied thereto a logic "1" write control voltage but for which the actual written state of such memory cells is sensed to be below a threshold voltage, i.e. it is sensed that such memory cells are insufficiently written, the write control data stored in the latch is maintained at the logic "1" level for further continued writing to such memory cells whereby further charge can be stored on the floating gate of such memory cells. For those memory cells having write control data initially set at a logic "0" state, those cells are never written into and remain in the erased state throughout the programming operation. Appendix A attached hereto summarizes the data modification rule and corresponding logical relationship according to the present invention by which writing of data to respective memory cells is controlled according to the present invention. It is Applicants' view that the writing of data according to the predetermined logical relationship taking into consideration both the actual written state of the memory cell and the write control data,

for which Applicants seek patent protection by way of the pending amended claims, is novel and nonobvious over the applied prior art.

Returning now to considerations of the prior art, it is believed that a brief review of various types of memories may be helpful in the evaluation of the pending amended claims. Therefore, Applicants would like to explain differences between ROMs, EPROMs, and EEPROMs.

ROM:

A ROM is a memory whose data can be read but not erased or rewritten. The method of storing data in the ROM is roughly divided into two types. One type is to store data in the process of manufacturing the ROM, and its typical example is a Mask ROM. For example, this type can be compared to a method of printing blank paper to bind the paper for a book. The other type is to store data in the ROM by a user, and the stored data is neither erased nor rewritten. Its typical example is a One Time Programmable ROM. The latter type can be compared to a method of engraving design on a flat plate with chisels by an engraver.

A ROM is directly connected to a processing unit of a computer system to store data proper to the computer system. For example, the ROM stores data as to what structure the computer system has, data as to how the system is operated after it is turned on, and the like.

As computer systems were updated, the data in the ROM was required to be rewritten, and an EPROM (Electrically Programmable ROM) was invented accordingly.

EPROM:

Since an EPROM is employed for the same purpose as that of the above-described ROM, the data in the EPROM is not usually rewritten. The need to rewrite data in the EPROM was arisen as computer systems were updated. The rewrite operations of the EPROM are performed several times to several tens of time, as follows:

1) Erase

The EPROM is detached from a computer, i.e., an EPROM socket and then irradiated with ultraviolet rays. The package of the EPROM is provided with a glass window, and the ultraviolet rays are emitted to internal silicon chips through the glass window, with the result that data is erased by the ultraviolet rays.

2) Program

The EPROM is mounted on a ROM writer by which new data is written. The data is written to each address byte by byte. Whenever data of one byte is written to an address, it is verified whether it is done correctly. If the data is written correctly, the next one-byte data is written to another address. If not, the same data is written again to the same address. The write and verifying operations are repeated until the data is written correctly. If data is written to all addresses, the rewrite operation of the EPROM is completed.

The EPROM whose data has been rewritten, is mounted again on the updated computer, i.e., the EPROM socket, and used like a ROM.

EEPROM:

The foregoing EPROM has the following drawbacks. To rewrite data, the EPROM has to be removed from the EPROM socket, and both an ultraviolet ray irradiating device and a ROM writer are needed in addition to the EPROM. Since the number of rewrite operations has recently been increased in accordance with the diversification of computer systems, the EPROM is inconvenient. Furthermore, the glass window of the package increases the cost of the EPROM.

An EEPROM (Electrically Erasable Programmable ROM) was invented in order to eliminate the above drawbacks of the EPROM. In particular, a batch erasing type EEPROM (flash memory), which can be manufactured at low cost, was invented as the very device by which the EPROM can be replaced. The flash memory has only to be on-board even when data is erased or rewritten, and needs neither an ultraviolet ray irradiating device nor a ROM writer. Moreover, no glass windows are necessary for the package of the EPROM.

In recent years, the EPROM is disappearing according to the diversification of computer systems and inexpensiveness of flash memories.

Regarding the IBM Bulletin applied in the parent application, as entitled "EPROM PROGRAMMING DEVICE", this reference relates to a device for writing data to an EPROM and, more specifically, to a personal computer. since the personal computer includes a ROM writer and an EPROM socket which is disposed on the back of the computer, data can be rewritten easily without removing an EPROM from the computer.

The personal computer requires an ultraviolet ray irradiating device to erase data; however, if the device is placed behind the computer, the EPROM needs not be removed therefrom. The IBM Bulletin is not directed to a new method of writing data to an EPROM but to a new personal computer that is disclosed in the Bulletin.

The figure of the IBM Bulletin shows a circuit arrangement of an adapter and a card-like ROM writer which are added to the personal computer. Otherwise, the IBM Bulletin is deficient for the reasons noted in the Amendment filed April 3, 1995. It is respectfully submitted that the IBM Bulletin does not teach latching write control data into data cells corresponding to respective memory cells and does not teach the predetermined logical operation as above described and as recited in Applicants' amended claims, by which programming of the memory cells is achieved while nevertheless avoiding overwriting of data in the memory cells. The difference is shown in Exhibit B attached to the Preliminary Amendment filed April 3, 1995.

For the reasons as noted in the April 3, 1995 Preliminary Amendment, the deficiencies in the IBM Bulletin are not believed to be remedied by the other applied references stated in the outstanding rejection in the parent application, and therefore the pending amended claims are believed to be patentably distinguishing over the prior art of record.

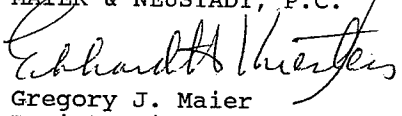
Also concurrently filed herewith is an Information Disclosure Statement making of record additional information, including commonly owned patents and pending applications, and

prior art cited therein, for consideration by the Examiner in the present application. The Examiner is particularly requested to review the claims pending in commonly owned U.S. Patent Application Serial No. 08/277,514 filed July 19, 1994, as well as the claims in commonly owned U.S. Patent 5,361,227 and 5,357,462. While Applicants have attempted to maintain a clear line of demarcation between the claims of the present application and the claims of Serial No. 08/277,514 and the '227 and '462 patents, the Examiner is respectfully requested to confirm that a clear line of demarkation in the claims has been made.

Accordingly, in light of the newly submitted claims, and in view of the above discussion, the newly submitted claims are believed patentably distinguishing over the prior art applied in the parent application, and in condition for allowance. An early and favorable action to that effect is therefore respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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----- DATA MODIFICATION RULE -----

	CASE 1-a	CASE 1-b	CASE 2-a	CASE 2-b
WRITE CONTROL DATA	1	1	0	0
STATE OF CELL	0	1	0	1
MODIFIED WRITE CONTROL DATA	1	0	0	0

*** case 1-a ***
In the case that "1"-write control data is initially set into the data circuit, the states of corresponding cell moves toward "1"-state from "0"-state. During the state of concerned cell stays in "0"-state, the next write control data for the next write operation must be "1"-write control data again.

*** case 1-b ***
In the case that "1"-write control data is initially set into the data circuit, the states of corresponding cell moves toward "1"-state from "0"-state. When concerned cell reaches the "1"-state, the write control data must be modified to "0"-write control data from "1"-write control data in order to inhibit over-programming. Therefore, the next write control data for the next write control data is "0"-write control data.

*** case 2-a ***
In the case that "0"-write control data is initially set into the data circuit, the state of corresponding cell is not changed. So, the corresponding cell remains in "0"-state. In this case, "0"-data must be memorized into the cell. Therefore, initial "0"-write control data is kept until the program operation is completed.

*** case 2-b ***
In the case that "0"-write control data modified from initial "1"-write control data is set into the data circuit, the state of concerned cell already stay in "1"-state. "0"-write control data in this case is set to inhibit the over-programming of cell which already stay in "1"-state. Therefore, "0"-write control data modified from initial "1"-write control data is kept until the program operation is completed.

----- EXAMPLE ----

	CELL 1	CELL2	CELL3	CELL4
INITIAL CONTROL DATA	0	0	1	1
INITIAL STATE OF CELL	0	0	0	0
After 1st WRITE OPERATION				
CONTROL DATA	0 (CASE 2-a)	0 (CASE 2-a)	1 (CASE 1-b)	1 (CASE 1-a)
STATE OF CELL	0	0	1	0
MODIFIED CONTROL DATA	0	0	0	1
After 2nd WRITE OPERATION				
CONTROL DATA	0 (2-a)	0 (2-a)	0 (CASE 2-b)	1 (1-b)
STATE OF CELL	0	0	1	1
MODIFIED CONTROL DATA	0	0	0	0

PROGRAMMING IS COMPLETED!! and
"0"-data is memorized CELL 1 and 2.
"1"-data is memorized CELL 3 and 4.

APPENDIX A